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Optimal Placement of Fuzzy based Nonal Switched UPQC Topology with Distributed Generation for the Power Quality Enhancement in IEEE 14 Bus System

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Abstract

An Unified Power Quality Conditioner (UPQC), owning the integration of shunt and series Active Power Filter (APF), has become a standard accepted solution in the area of current and voltage harmonics mitigation of a power system network. This paper furnishes a novel approach of nonal switched UPQC topology, supported with Distributed Generation (DG), aiming at the power quality enhancement and position optimization, placed at different locations in a standard IEEE 14 bus system. In addition to this, the behaviour of the proposed topology is analysed using Fuzzy Logic and Space Vector Pulse Width Modulation (SVPWM) as control algorithms and the outcomes are compared with the historical twelve switch UPQC topology. Simulation results of the proposal modelled in MATLAB/SIMULINK reveals the superiority of nonal switch UPQC and the optimal position of the proposed conditioner, for mitigating the harmonic issues in the standard IEEE 14 bus system

Keywords: Fuzzy Logic Controller (FLC), IEEE 14 Bus System, Nonal Switch UPQC, Power Quality (PQ), SVPWM

1. Introduction

In the current booming world, survival is inconceivable without the usage of electric power. Hence electrical energy plays a leading role. Assisting this, it is essential to promote the uninterrupted sustainable quality of electrical power to the end user, as many customer loads mandates the continual distortion free supply. But, the usage of soft switching devices and the nonlinear loads in the power system causes heating, harmonics, flickers and many other disturbances which will impact the system's availability and reliability.

To dilute the power quality issues, power quality monitoring equipment and power quality conditioners should be lodged in the distribution side to curb the harmonics, voltage sags, voltage swell, etc.

Rahul Virmani presented a work on the "Performance Comparison of UPQC and Active Power Filters for a Non-Linear Load". This work transparently remarks the advantages of implementing the UPQC into the power system, when compared with an APF. The control algorithm is recommended to diminish the harmonics, but with the need of excessive memory consumption[1].

The research titled "A Low Cost High Performance UPQC for Current and Voltage Harmonics Compensations" carried out by Quoc-Nam from Korea, suggest the use of low cost, high performing UPQC devices in a power system. They further proposed that the insertion of a capacitor in succession to shunt APF, will considerably curtail the voltage across the DC link[2].

Mohammed Abdul Ahad Yahiya's work on "Performance Analysis of DVR, DSTATCOM and UPQC

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for Improving the Power Quality with Various Control Strategies" compares the voltage quality enhancement techniques implemented using DVR, D-STATCOM and UPQC, actuated with PI controller and FLC, but are computationally rigorous because of the complex algorithm with inefficient memory management[3].

Vinod Khadkikar revealed a new comprehensive review on the divergent possible UPQC topologies for single and three phase networks, to enhance the power quality[4].

Supplementing these, few conventional solutions for power quality improvement were still debatable due to inefficient algorithms, over consumption of memory and less impact on harmonics. Addressing these, there are noticeable advancements attempted in the literatures[5–11].

In this proposed methodology, the nonal switched UPQC topology is implemented along with DG, implanted in different locations of an IEEE 14 bus system which are controlled with the FLC and SVPWM control algorithms. Supporting this, the results are contrasted with twelve switch UPQC topology with the same stated control strategies. The simulation results, proving its effectiveness in harmonics reduction at different optimal location are presented.

The remainder of the proposed work is arranged as follows. Section 2 evokes the control strategies implemented in this research for UPQC. The detailed UPQC Configurations are given in Section 3. Section 4 presents the IEEE 14 Bus system. Section 5 documents the simulation results, and the conclusion of this work is reported in the Section 6.

2. Control Strategy

The key idea of control strategy is to calculate and facilitate the injection of required quantity of the voltage and current signals to improvise the compensation effect in the system. To accomplish this, FLC and SVPWM are proposed in this research.

2.1 FLC Control Strategy

The modular layout of FLC is a composition of Fuzzification, Inference engine, Defuzzification blocks[12].

The approach of restyling the input/output variable to linguistic labels is entitled as fuzzification. In the proposed methodology, 07 classes of linguistic labels namely: Large Positive (LP), Medium Positive (MP), Small Positive (SP), Zero (ZE), Small Negative (SN), Medium Negative (MN), Large Negative (LN) projected over there membership grades are used, to decompose each system variable into fuzzy regions having the range [-1 1].

Inference Engine: The performance of the FLC, relating the input and output variables of the system is influenced by a set of rules. These rules relating the error and its rate of change are depicted in Table 1. Based on this, 49 rules are formed and are designated as the Knowledge repository of the FLC.

Defuzzification: The fuzzy set has to be altered into crisp solution variable before it can be used to control the system. This is realized by using a defuzzifier block.

Error \ Rate of change of error	LP	MP	SP	ZE	SN	MN	LN
LN	ZE	SP	MP	MP	LP	LP	LP
MN	SN	ZE	SP	MP	MP	MP	LP
SN	MN	SN	ZE	SP	SP	MP	LP
ZE	MN	MN	SN	ZE	SP	MP	MP
SP	LN	MN	SN	SN	ZE	SP	MP
MP	LN	MN	MN	MN	SN	ZE	SP
LP	LN	LN	LN	MN	MN	SN	ZE

Table 1. Fuzzy control rules

2.2 SVPWM Control Strategy

The execution structure of SVPWM involves conversion of signals form a, b, c frame to d-q frame and further from d-q frame to a, b, c frame. It effectively utilizes the space vector theory to calculate the duty cycle and finally to generate the gate pulse for APF.

The advantages offered by the implemented SVPWM control strategy are low switching loss, less THD in the spectrum of switching waveform, low implementation complexity and reduced computational difficulties with optimal memory consumption.

3. UPQC Configurations

In this section, two configurations of 3-ϕ UPQC systems, used to mitigate the power quality complications, are described.

The Figure 1 represents the general outline of UPQC. It is comprised of two 3-ϕ active voltage source inverter filters namely Series Active Filter (SAF) and Parallel

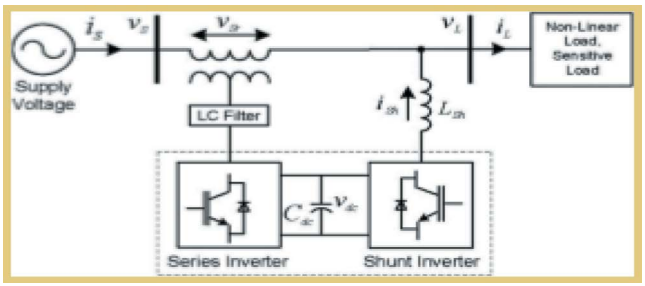

Figure 1. General structure of UPQC.

Active Filter (PAF), associated in sequence with a common DC Link. The SAF is in series with the line and operates to compensate the voltage quality problem in the line. The PAF is in shunt to the line aiming to compensate the current quality problem in the line and to regulate the DC link. Figure 2 depicts the 3P3W VSI-based UPQC topology involving 12 switches, ultimately feeding 3P3W load. This is the most widely used and commonly studied configuration.

In addition to this, a novel topology named 3P3W VSI-based UPQC topology involving 9 switches is proposed, which is as described in the Figure 3. The switch count has been reduced by 33% than the historical 12 switch UPQC topology, without considerably sacrificing in the ideal performance.

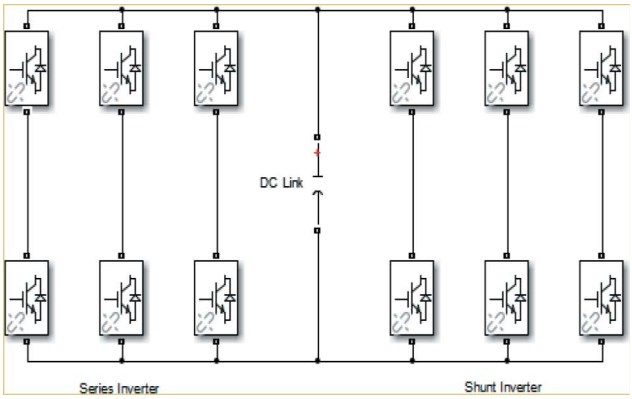

Figure 2. 3P3W UPQC topology with 12 switches.

4. IEEE 14 Bus System

Single line layout of standard IEEE 14-Bus system is showcased in the Figure 4 with loads presumed to be with constant impedance and all generators run with constant mechanical power input and with fixed excitation. It composes of 05 number of synchronous rotating

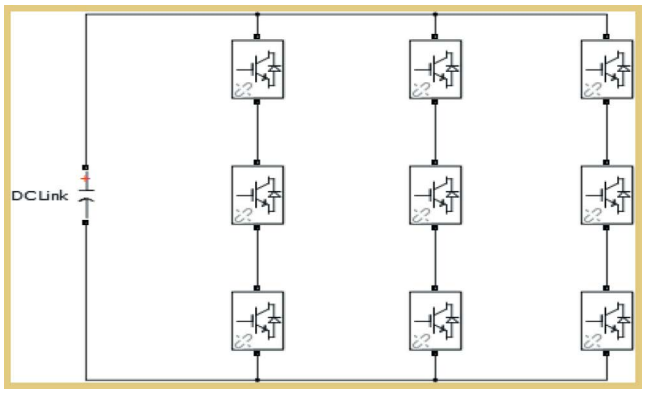

Figure 3. 3P3W UPQC topology with 9 switches.

devices with IEEE type-1exciters, 03 number of them are synchronous compensators used only for reactive power support with generator 1 considered as a reference generator.

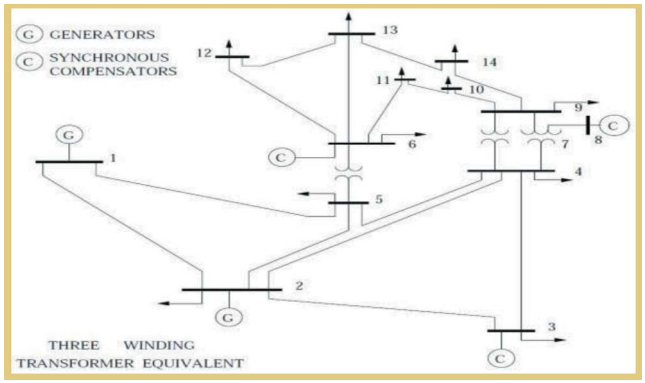

Figure 4. IEEE 14 bus test system.

5. IEEE 14 Bus System

To enable the comparative harmonic analysis of the two stated UPQC configurations gated with two control strategies namely FLC and SVPWM and to optimize their location, the proposed UPQC models are constructed in the MATLAB/SIMULINK environment. The Figure 5 shows the detailed SIMULINK model of a 3P3W UPQC configuration, fired with FLC. It consists of a 3-ϕ voltage source rated 400V, 50Hz feeding a critical 3-ϕ load through the power transformers and transmission line.

The SAF and PAF are realized using IGBT bridge circuit with 12 switches. The 3-ϕ to ground fault having short circuit transition time of [0.15-0.3] s, is also simulated. Similarly, the other proposed configuration namely 9 switches topology is also modeled in the SIMULINK and successfully executed. The UPQC models are placed in between all the branches of an IEEE 14

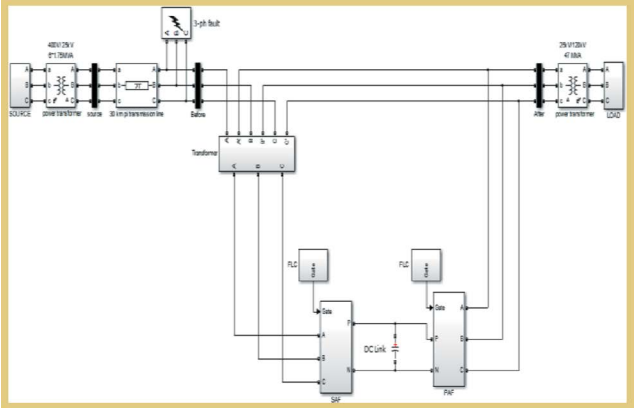

Figure 5. Simulink model of 3P3W UPQC configuration.

Bus system. The UPQC are gated through FLC and SVPWM separately and the harmonic analysis of voltage and current waveforms, (for phase A), measured before compensation and after compensation for both the two stated UPQC configurations are accomplished and the results are processed through the harmonic FFT analysis.

Figure 6 depicts the waveforms of voltage before compensation and after compensation and Figure 7 represents the current waveforms before compensation and after compensation for 3P3W configuration, placed between Bus 1 and Bus 2 of IEEE 14 Bus system. Both the figures indicating three phase waveforms in phases A, B and C are represented by the red, blue and green lines respectively.

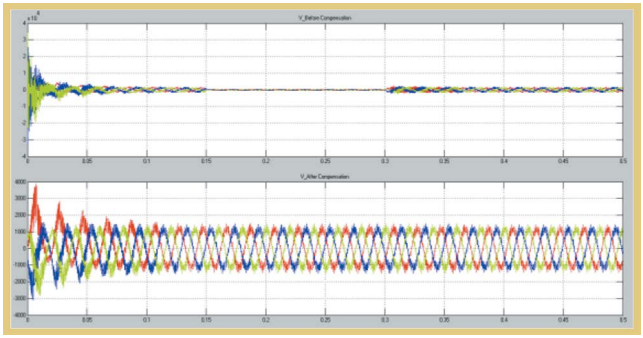

Figure 6. Simulated results of voltage waveforms.

The harmonic data of 3P3W topology with 12 switches controlled with FLC and SVPWM, placed between all the branches of IEEE 14 Bus system are summarized in the bar charts depicted as Figures 8 and 9 respectively.

Similarly, the harmonic data of 3P3W topology with 9 switches controlled with FLC and SVPWM, placed between all the branches of IEEE 14 Bus system are summarized in the bar charts depicted as Figures 10 and 11 respectively.

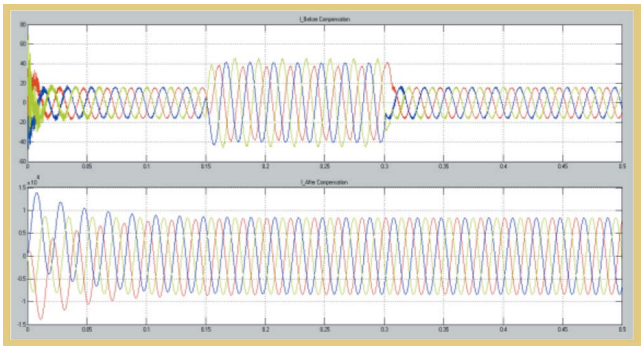

Figure 7. Simulated results of current waveforms.

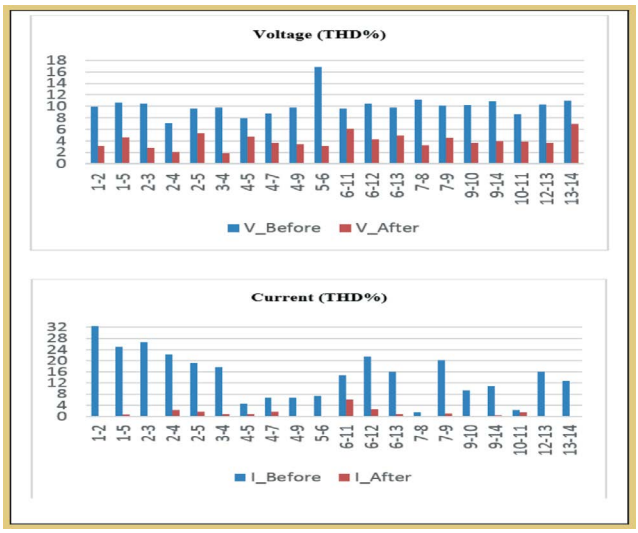

Figure 8. Harmonic data of 3P3W topology with 12 switches and FLC.

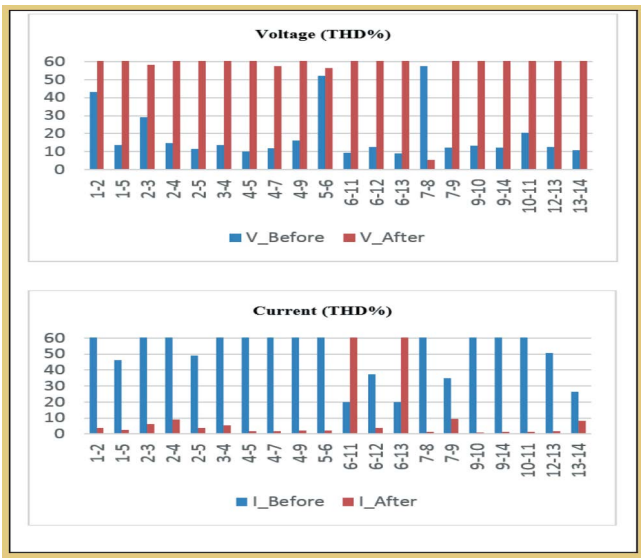

Figure 9. Harmonic data of 3P3W topology with 12 switches and SVPWM.

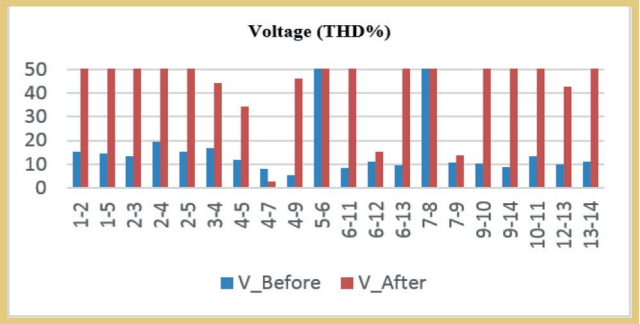

Figure 10. Harmonic data of 3P3W topology with 9 switches and FLC.

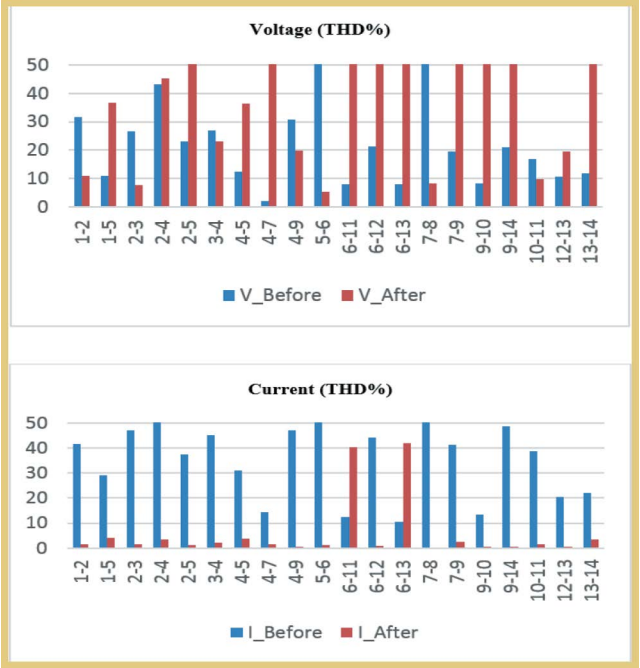

Figure 11. Harmonic data of 3P3W topology with 9 switches and SVPWM.

6. Conclusions

Power quality issues such as voltage swell and sag are most commonly occurred in the power distribution system. To overcome these issues, different topologies of UPQC are proposed in this paper. To enhance the power quality, 12 switch UPQC with fuzzy logic controller and 12 switch UPQC with space vector pulse width modulation, are implemented in MATLAB Simulink to minimize the voltage sag under different configurations. Further, the results of above stated configurations are compared with the novel 9 switch UPQC with fuzzy logic controller and 9 switch UPQC with space vector pulse width modulation configurations, which are also simulated.

From the harmonic analysis, it is clearly indicated that the for 3P3W UPQC topology with 12 switches and gated with FLC, placing the UPQC in between bus 3 and bus 4 will be the optimal location, where both the voltage and current harmonic level can be drastically reduced to 1.87% and 0.82% respectively. If current harmonic is of concern, then the placing the UPQC in between bus 7 and bus 8 is an optimal choice, where the current harmonic level is reduced to 0.07%.

For 3P3W UPQC configuration with 12 switches and gated with SVPWM, placing the UPQC in between bus 7 and bus 8 will be the optimal placement, where the voltage harmonic level can be managed to 5.43% and current harmonic level can be controlled to 1.16%. If current harmonic is of interest, then the placing the UPQC in between bus 9 and bus 10 is an optimal choice, where the current harmonic level is reduced to 0.85%.

Similarly, for 3P3W UPQC topology with 9 switches and gated with FLC, placing the UPQC in between bus 4 and bus 7 will be the optimized position of placement, where the voltage and current harmonic level can be quenched to 2.85% and 0.75% respectively. If current harmonic is of importance, then the placing the UPQC in between bus 9 and bus 10 is an optimal one, where the current harmonic level is reduced to 0.17%.

Likely, for 3P3W topology with 9 switches and gated with SVPWM, placing the UPQC in between bus 5 and bus 6 will be the optimized target, where both the voltage and current harmonic level can be hindered to 5.32% and 1.37% respectively. If current harmonic is of concern, then the placing the UPQC in between bus 7 and bus 8 is an optimal choice, where the current harmonic level is reduced to 0.43%.

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