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An FPGA Based Single Phase Multilevel Inverter

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This work presents a new multilevel inverter topology using an H-bridge with bidirectional auxiliary switch, eight diodes and two capacitors to get five level ac output. It presents an FPGA based gate signal generator for multilevel inverter to control its output voltage. The XILINX FPGA based multilevel inverter is chosen for the hardware implementation of switching strategy mainly due to its high computation speed that can ensure the accuracy of the instants that gating signals are generated. Spartan 6 board is used to get hardware output and these results are validated with simulated results.

Keywords: *H-Bridge Inverter, Auxiliary switch, FPGA.*

1.0 INTRODUCTION

The various types of multilevel inverter topologies presented in [1] show a number of characteristics in common, giving them some clear advantages over bi-level converters, like reduction in the commutation frequency applied to the power components, reduction in the voltages applied to the main power switches, enabling operation at higher load voltages and transient voltages automatically limited in [2].

The main drawback associated with the multilevel inverters is their circuit complexity, requiring a high number of power switches [3]. They also require a more number of auxiliary dc levels, provided either by independent supplies or, more commonly, by a cumbersome array of capacitive voltage dividers. In this case, ensuring that the dc voltages are kept in equilibrium is another factor that increases the complexity of the modulator circuit.

This work proposes a new converter topology, presented in Figure 1. This topology includes an H-bridge with an auxiliary bidirectional switch, diodes, capacitor and power supply. This topology is used in the design of the five-level DC-AC inverter output presented below. The design requires five switches whose gates has to be driven by five different pulses with different pulse width according to the calculation done for the same.The pulses are generated through Field Programmable Gate Arrays (FPGAs). They are considered as an appropriate solution in order to boost the performance of controllers used in [4].

FPGA technology is now considered by an increasing number of designers in various fields of application such as wired and wireless telecommunications in [5], image and signal processing used in [6], where the always more demanding data throughputs take advantage of the ever increasing density of the chips. Still, more recently, other application fields are in growing demand, such as medical equipment in [7], robotics in [8,9], automotive in [10] and space and aircraft embedded control systems in [11]. Industrial electrical control systems are also of great interest because of the ever increasing level of expected performance in [12].

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This paper presents procedure for generation of pulses for five level inverter using FPGA. It also shows hardware implementation of five level inverter using FPGA controller.

2.0 SIGNAL GENERATION USING FPGA

Traditionally, mathematical models have been developed to evaluate the functionality of global engineering systems. However, the practical development of each part of the system needs then to be separately addressed. This often involves the use of other CAD tools and/or different software platforms, with the design itself being developed in a different environment. Recent advance in CAD methodologies / languages used in [13] has brought the functional description of design and practical hardware implementation closer. System level modeling languages (such as Handel-C, System-C) and Hardware Description Languages (such as VHDL, Verilog) [14] enable the underpinning mathematical description and the electronic design implementation to be simultaneously addressed in a unique environment, supported by a range of major Computer Aided Engineering platforms. Synthesis tools can compile such designs into a variety of target technologies.

A holistic system level approach to the design and development of an electronic system enables a top-down design methodology in [15], which begins with modeling an idea at an abstract level, and proceeds through the iterative steps necessary to further refine this into a detailed system. A test environment is developed early in the design cycle. As the design evolves to completion, the language is able to support a complex detailed digital system description and the test environment will check compliance with the original specification. Concepts are tested before investment is made in hardware / physical implementation.

2.1 FPGA design flow

Design entry is an electronic design automation that encapsulates a circuit description from [16]. It captures a design and prepares it for simulation. Design requirements dictate the type of design capture tool as well as the options needed. Some of the options would be:

- Schematic capture
- Hardware Description Language (HDL) capture:
- Very high speed integrated circuit Hardware Description Language for short VHDL
- And Verilog: language for purely numerical description that mixes structural and algorithmic description.

Functional verification confirms that the functionality of a circuit model conforms to the intended or specified behavior, by simulation or by formal verification methods. There are two major tool sets for simulation: Functional (Logic) simulation tools and Timing simulation tools.

Functional simulators verify the logical behavior of a design based on design entry. Timing simulators perform timing verifications at multiple stages of the design. In this simulation the real behavior of the system is verified when encountering the circuit delays and circuit elements in actual device. In general, the simulation information reflects the actual length of the device interconnects.

Once the FPGA design is created and verified, Synthesis process will translate abstract descriptions of functionality such as HDL into optimal physical realizations, creating net lists that can be passed to a place and route tool specifying how the components should be wired together as in [17]. Then, the designer maps the gate level description or net list to the target design library and optimizes for speed, area or power consumption.

In this last verification step, the bit stream file is fed to a simulator to simulate the design functionality in [16] and report errors in the real environment's desired behaviour. Timing tools are used to determine maximum clock frequency of the design.

After design verification the code is dumped into FPGA board, finally output pulses from FPGA are given to inverter hardware circuit.

3.0 POWER STAGE

3.1 Circuit Configuration

Figure 1 shows the complete power circuit used in the five-level inverter. The H-bridge is formed by the four main power devices, S1 to S4 and four diodes D1 to D4. A capacitor voltage divider, formed by C1 and C2 in [18] provides a half supply voltage point, node A in Figure 1. The auxiliary switch, formed by the controlled switch S5 and the four diodes, D5 to D8, connects the centre point of the left hand half-bridge to node A.

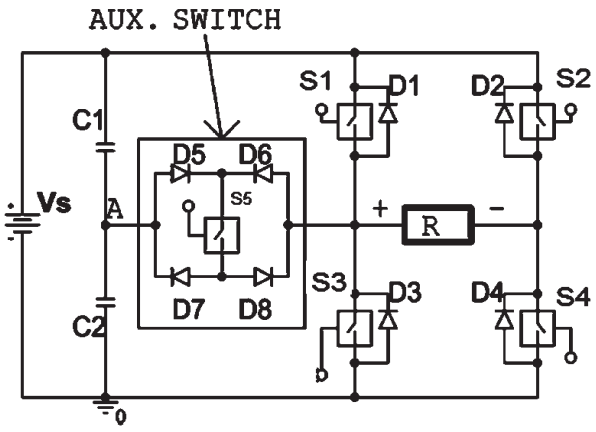


FIG. 1. H-BRIDGE INVERTER WITH BIDIRECTIONAL SWITCH

3.2 Stage Advantages

The number of components required to implement a five-level inverter using the new topology and other three multi-level inverters can be compare through:

A) Main power switches

The new topology achieves a 37.5% reduction in the number of main power switches required, using only five controlled power switches instead of the eight required in any of the other three configurations. The auxiliary switch voltage and current ratings are lower than the ones required by the main controlled switches.

B) Auxiliary devices (diodes and capacitors)

The new configuration reduces the number of diodes by 60% (eight instead of 20) and the number of capacitors by 50% (two instead of four) when compared with the diode clamped configuration. The new configuration reduces the number of capacitors by 80% (two instead of 10) when compared with the capacitor clamped configuration.

Additionally, since the two capacitors are connected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation, avoiding a problem that can limit operating range in some other multilevel configurations.

C) Power Stage Operation

The required five voltage output levels (Vs, Vs/2, 0, -Vs/2, -Vs) are generated as follows:

a) Maximum positive output, Vs

S1 is ON, connecting the load positive terminal to Vs, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vs. Figure 2 shows the current paths that are active at this stage.

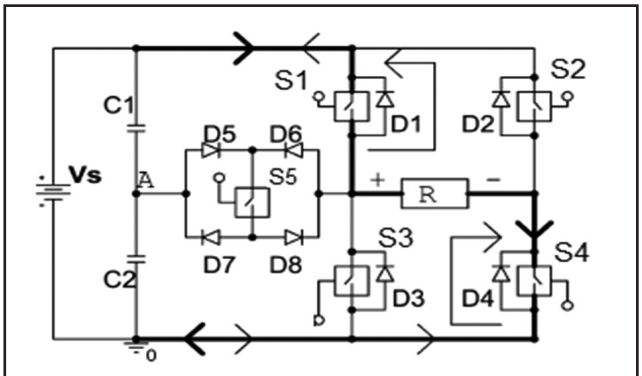


FIG. 2. SWITCHING COMBINATION REQUIRED TO GENERATE OUTPUT VOLTAGE LEVEL VS/2

b) Half-level positive output, Vs/2

The auxiliary switch, S5 is ON, connecting the load positive terminal to point A, through diodes D5 and D8, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vs/2. Figure 3 shows the current paths that are active at this stage.

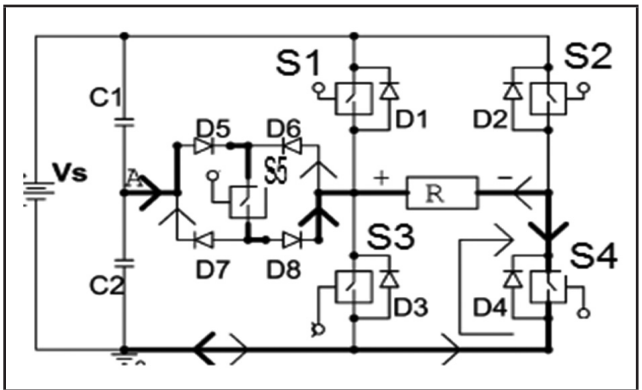


FIG. 3. SWITCHING COMBINATION REQUIRED TO GENERATE OUTPUT VOLTAGE LEVEL VS/2

c) Zero output

The two main switches S3 and S4 are ON, short-circuiting the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero. Figure 4 shows the current paths that are active at this stage.

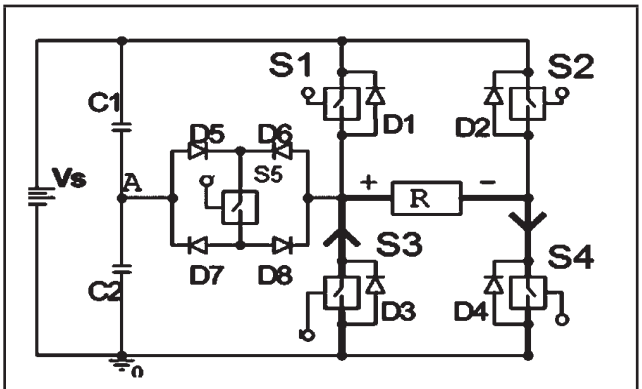


FIG. 4. SWITCHING COMBINATION REQUIRED TO GENERATE OUTPUT VOLTAGE LEVEL VS/2

d) Half-level negative output, -Vs/2

The auxiliary switch, S5 is ON, connecting the load positive terminal to point A, through diodes D6 and D7, and S2 is ON, connecting the load negative terminal to Vs. All other controlled switches are OFF; the voltage applied to the load terminals is –Vs/2. Figure 5 shows the current paths that are active at this stage.

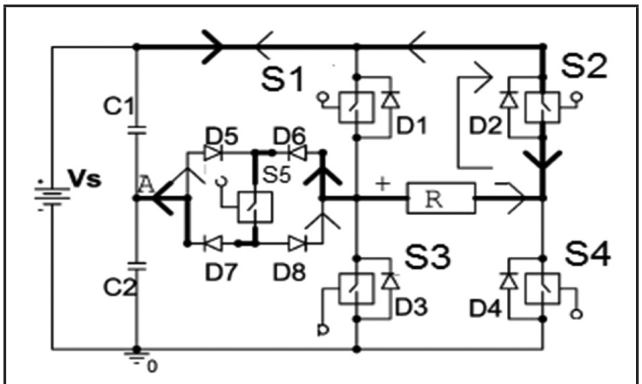


FIG.5. SWITCHING COMBINATION REQUIRED TO GENERATE OUTPUT VOLTAGE LEVEL VS/2

e) Maximum negative output

S2 is ON, connecting the load negative terminal to Vs, and S3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is (-Vs). Figure 6 shows the current paths that are active at this stage.

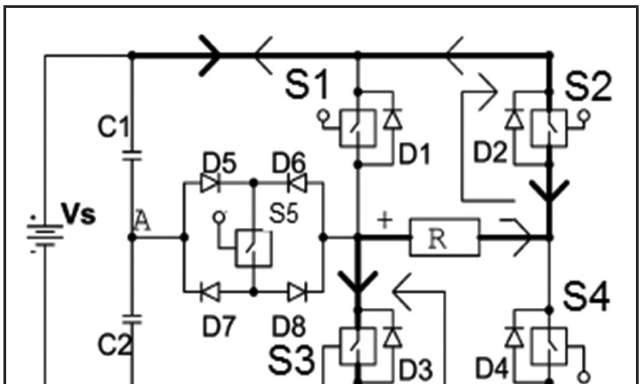


FIG.6 SWITCHING COMBINATION REQUIRED TO GENERATE OUTPUT VOLTAGE LEVEL VS/2

Table I lists the switching combinations that generate the required five output levels (Vs, Vs/2, 0, -Vs/2, -Vs). In this configuration the two capacitors in the capacitive voltage divider are connected directly across the dc bus, and since all

switching combinations are activated in an output cycle, the dynamic voltage balance between the two capacitors is automatically restored.

TABLE 1

SWITCHING COMBINATIONS REQUIRED TO GENERATE FIVE LEVEL OUTPUT WAVEFORM.

S_1	S_2	S_3	S_4	S_5	V_{RL}
on	off	off	on	off	V_S
off	off	off	on	on	$V_S/2$
off	off	on	on	off	0
off	on	off	off	on	$-V_S/2$
off	on	on	off	off	$-V_S$

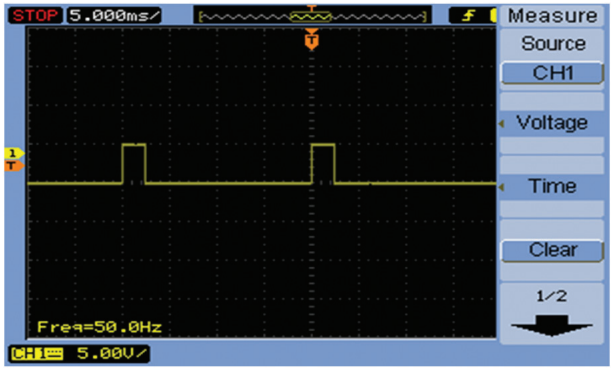
4.0 HARDWARE RESULTS

The VHDL code for new multilevel single phase inverter written in Xilinx software and is simulated by using ModelSim. The generated pulses from FPGA Spartan 6 board which are observed in CRO are shown in Figure 7. These pulses are given to five level inverter. Hardware results are shown in Table 2. Figure 8 shows output waveforms. Main components used in the circuit and their ratings are given in Table 3 .

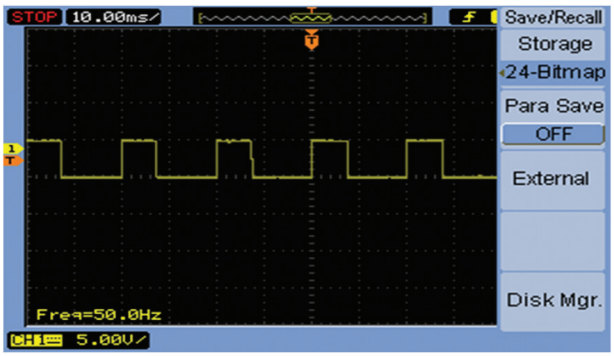
TABLE 2

OUTPUT VOLTAGE AND CURRENTS FOR DIFFERENT INPUT VOLTAGES

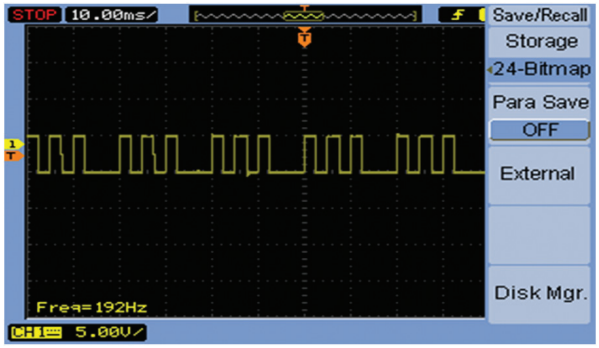
S. No	Input Voltage (V)	Output voltage (V)	Output current (A)
1	230	200	0.187
2	100	82.2	0.1



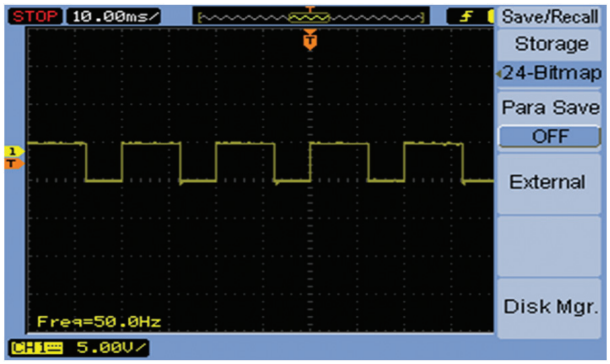
(a)



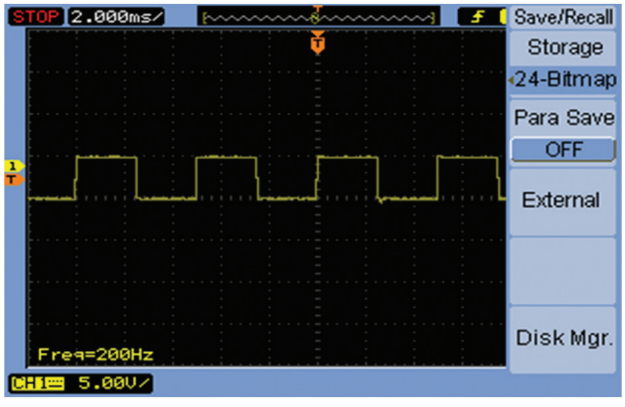
(b)



(c)

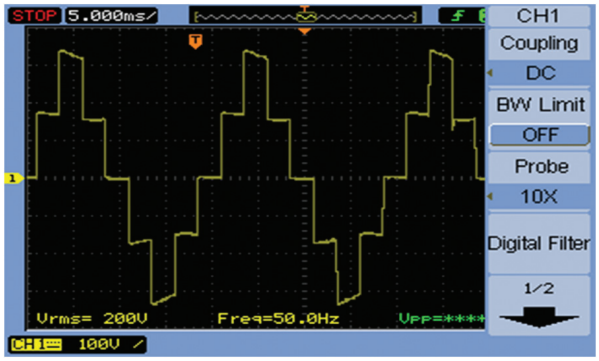


(d)

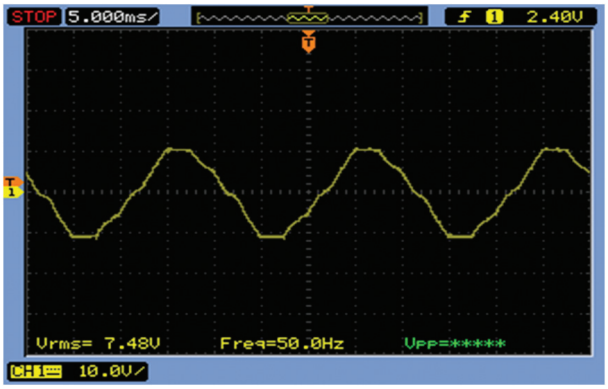


(e)

FIG. 7. SWITCHING PULSES FOR FIVE DEVICES (A) SWITCH 1 (B) SWITCH 2 (C) SWITCH 3 (D) SWITCH 4 (E) SWITCH 5



(a)



(b)

FIG.8. (A) OUTPUT VOLTAGE, (B) OUTPUT CURRENT

TABLE 3

COMPONENTS USED IN THE CIRCUIT AND THEIR RATINGS

S. NO	COMPONENT NAME	RATING
1	Bridge rectifier	600V, 35A
2	IGBT (FGA25N/120)	I_{max} = 25A V_{max}=1200V
3	Diode (MUR 30/20)	I_{max} = 25A V_{max}=1200V
4	C1, C2	1000uf / 450V

5.0 CONCLUSION

The new multilevel topology with the bidirectional auxiliary switch produced the required five-level output using only five power switches, and only one centre tap provided by two capacitors. A prototype model is developed for it, the gate pulses are provided through FPGA.

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