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DSP-controlled laboratory prototype of 4 bus rds with DSTATCOM for voltage regulation

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This paper reports the development of a prototype of 4 bus Radial Distribution System (RDS) with shunt connected Distribution Static Var Compensator (DSTATCOM) capable of voltage regulation. Digital signal processor TMS320F2812^{TM} is selected due to its analog/digital input-output compatibility, high speed and cost effective. Use of PI Controlled inverter as the power stage of the Voltage Source Controlled (VSC) based DSTATCOM generates required compensation to improve voltage regulation. The experimental studies are carried out and results are discussed.

Keywords: *DSTATCOM, Digital Signal Processor, Voltage Controller, Radial Distribution System.*

1.0 INTRODUCTION

An earthquake is the sudden, with an extensive use of digital systems in the field of production and controlling industry, the need for research in digital control of DSTATCOM has been increased. Digital Controller using a microprocessor can remotely monitor and control the internal parameters of the converters. It can change the operating condition without making change of hardware which results in a high performance controller [1-2].

At the same time these equipments are quite sensitive to deviations from the ideal sinusoidal line voltage. In such conditions both electric utilities and end users of electric power are more concerned about the quality of electric power. Conventional mitigation equipment is proving to be inadequate for an increasing number of applications. This fact has attracted the attention of power engineers to develop dynamic and adjustable solutions to power quality problems. Voltage Source Converter (VSC) based the DSTATCOM can be used for good voltage regulation and power factor correction. It is also used in distributed generation [3-4].

The control algorithms are based on instantaneous quantities such as p - q theory [5], I cosθ [6, 7], nonlinear control algorithm [8, 9], direct power control [10, 11], model predictive control [12], Instantaneous reactive power theory [13], least mean square algorithm[14] under ideal and distorted ac mains. These are implemented in three phase three - wire and four - wire balanced ac mains. Some of the new control techniques include adaptive filter [15] and composite observer based control algorithm [16] based on the state - space approach. The use of Adeline neural network based filtering scheme for extracting voltage components is reported in [17, 18]. In this paper phase shift control strategy is used, which includes familiar components such as Proportional Integral (PI) controllers and Sinusoidal Pulse-Width Modulation (SPWM). It is implemented by using TMS320F2812^{TM}.

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The digital controller performs well to maintain constant voltage magnitude at the load point.

2.0 SYSTEM CONFIGURATION

The block diagram for RDS with DSTATCOM is shown in Fig 1. The RDS line parameters are shown in the hardware

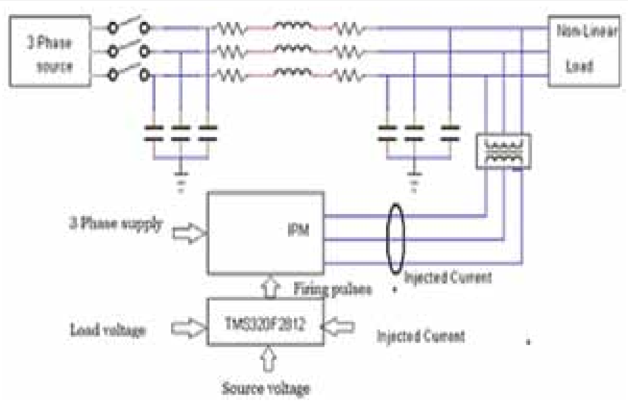

FIG.1 SCHEMATIC DIAGRAM OF DSTATCOM FOR 4 BUS RDS

implementation, first stage includes the conversion of power quantities i.e., 3-phase source voltages, dc link capacitor voltage, load currents and filter currents using Hall effect voltage and current transducers to low level signals preferably within the range of ±5 V. These signals from Hall Effect sensors are further conditioned using signal conditioning circuit to the range of 0-3 V, which is compatible with DSP 2812.

FIG.2 HARDWARE MODEL

The DSP 2812 is connected to the host computer through the parallel port. Code was developed using C language and after the code flashed in to the processor, the DSP- generated six gate pulses and that is connected to VSC which of control six IGBT switches in the IPM. The exchange of reactive power between the converter and the AC system can be controlled by varying the amplitude of the 3-phase output voltage. Hardware model is shown in figure 2.

3.0 DESCRIPTION OF HARDWARE

3.1 Control Systems

PI controlled Sinusoidal pulse-width modulation is a method used to control the switching of the IPM in the VSC. In proposed system, compare the 50 Hz, 3-phase sinusoidal voltage output of the control algorithm to a 10 kHz triangular waveform to yield the train of pulses required to produce a 50 Hz sinusoidal waveform at the output of the VSC. The PWM module of the DSP was a built-in function. The bulk of the work lied in enabling the appropriate control registers and configuring them such that the output of the module yields six pulse trains to drive the IPM. The duty cycle of the SPWM outputs were varied sinusoidally to produce a sinusoidally varying output of 50 Hz. This was accomplished by updating the PWM duty cycle register.

Unit tests of the SPWM module were performed by varying the duty cycle and observing the output. The input sinusoidal waveform is shown in Figure 3, overlaid with the resulting SPWM pulses produced by the DSP. The modulation index for this wave is 1 utilizing the full range on voltage input on the DSP. To aid in the design of the capacitor pre-charging circuit, system had to establish the logic of the SPWM output pulses that would be fed to the IPM. Table 1 shows a simplified truth table extracted from the IPM datasheet from Table 1, it was necessary for the DSP to feed to the IPM the exact same signal to each pair of complementary switches. The existence of the NOT gate was laterproved by the application guide.

The most widely implemented PLL method which employs a Zero-Crossing Detector (ZCD). The ZCD detects the positive transition zero crossing of the voltage and outputs a square pulse magnitude of 5 V. The time between each pulse is 20 ms - the period of a 50 Hz signal. Output a pulse is sent to the DSP executing the PLL algorithm to indicate a zero crossing, and to begin calculating angle Φ. In Time progresses Φ varies from 0 to 360□.

TABLE 1			
TRUTH TABLE			
SIGNAL TO LOW	SIGNAL TO HIGH	LOW SWITCH	HIGH SWITCH
H	L	Open	Open
L	L	Closed	Open
H	H	Closed	Open

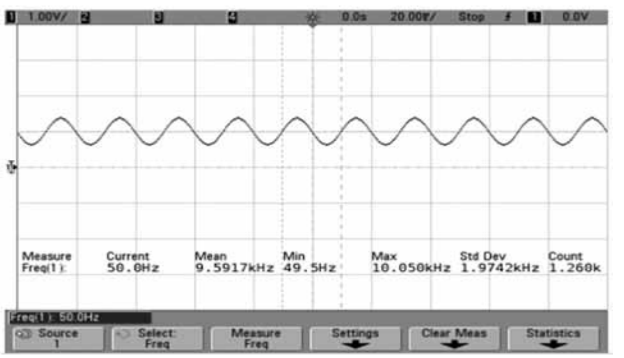

FIG.3 INPUT SINUSOIDAL WAVE FORM

The easiest way to generate a sinusoidal waveform is use the lookup table usually contains from 0 to 256 data.Once the lookup table values obtained from the table, they are multiplied by scaling values to determine the actual amplitude of the modulation output.

3.2 Distribution Systems

A Distribution Static Synchronous Compensator (DSTATCOM) used to compensate voltage sags on distribution network. In this paper to develop laboratory prototype considered 4 bus RDS model rating with 400 V, 7 A. with a length of 60 km to distribute power to loads as shown in figure 4. The distribution parameters are shown in Table 2.

TABLE 2		
RDS PARAMETERS		
SI. NO.	PERAMETER	VALUE
1	R- Resistance	2.5 Ω,7 A
2	L- Inductor	31.8 mH
3	C-Capacitor	0.22 µF,1500 V

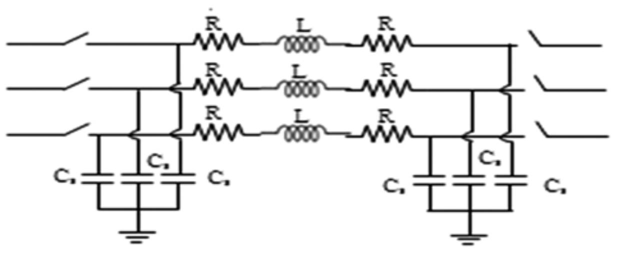
FIG.4 DISTRIBUTION SYSTEM MODEL

3.3 Voltage Source Converter

The Voltage Source Inverter (VSC) as shown in fig 5, is one of the main parts of the system and here Intelligent Power Module (IPM) is used as VSC. There are many advantages to use a module such as the IPM: it has an internal gate-driver which eliminates the need for us to design and build one externally, and the six IGBTs included in the IPM ensured that they were identical and no issues with manufacturing differences. The IPM also includes a configurable smart shutdown function which effectively disables the IPM in the event of an over current.

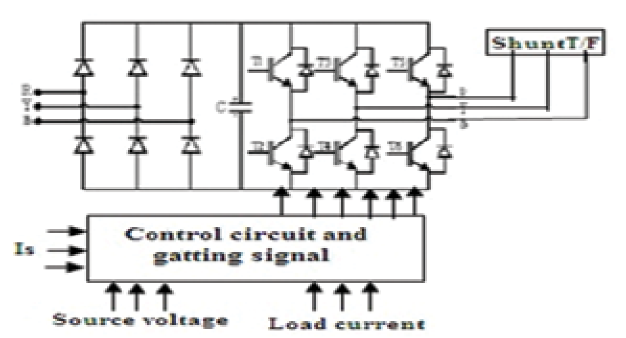

FIG.5 VOLTAGE SOURCE CONVERTER CIRCUIT IN IPM

3.4 Digital Signal Processing

A new approach of DSP controllers is becoming a viable option for even the most cost sensitive applications like FACTS systems etc. In addition to traditional mathematical functions like digital filter, FFT implementations, this new class of DSPs integrates all important modules in power electronics to simplify the system implementation. This integration lowers the overall part count of the system and reduces the board size. The TMS320F2812™, the first single-chip DSP solution for the digital control system market, integrates the TI 32 bit, fixed-point TMS320F2812™ DSP core with several microcontroller peripherals.

The DSP core itself has up to 150 MIPS (6.67 ns cycle time) speed and can execute the useful multiply/accumulate instruction in a single cycle. The DSP controller TMS320F2812™ from Texas Instruments is utilized to implement Voltage regulation of RDS. TMS320F2812™ has a 150 MIPS 16 bit fixed point DSP core. Which also integrates the following power electronics peripherals – 6 PWM channels three 16 bit multi-mode general purpose timers, 6 channel 12 bit ADC with simultaneous conversion capability, six capture pins, encoder interface capability, SCI, SPI, Watch Dog etc. 6 PWM channels (PWM1 through PWM6) control the three-phase voltage source inverter. These six PWM channels are grouped into three pairs (PWM 1&2, PWM 3&4, PWM 5&6). Three compare registers, called Full Compare, are associated with each PWM channel pair. Then the compare register values are updated to obtain the proper PWM output. The on chip software programmable dead band module provides adequate dead time to avoid shoot through fault.

4.0 RESULTS AND DISCUSSION

TABLE 3
EXPERIMENTAL SETUP PARAMETERS

Source voltage	125 V, 50 Hz Balanced Voltage
Load	0.75 KW induction motor and 3 KW, 4 A resistive load
DC Capacitor (c_1,c_2)	2200 µF, 400 V
DC voltage	300 V

To create under voltage condition, loading rheostat and an induction motor load is connected to the 4 Bus RDS which is being excited by a sinusoidal input. A heavy current drawn due to the motor direct-online (DOL) starting ability, has initiated under voltage as demonstrated in fig 6. The under voltage was compensated by activating DSTATCOM which injects currents into the Radial Distribution System. Fig 7 shows output under voltage due to load. The under voltage was compensated by activating DSTATCOM which injects currents into the Radial Distribution System. Fig 8 shows that after compensating under voltage in Load voltage, both source voltage and load voltage amplitudes are become equal . Due to induction motor load harmonics are introduce in to the system as shown in Fig 8 and the THD is 6.314 % when DSTATCOM activated the THD was reduced to 2.626% as shown in Fig 9 which improved the system performance of the system when DSTATCOM connected.

TABLE 4
RESULTS COMPARISON

S NO	1	2	3	4
Settling time(msec)	25	24	17.5	20
Peak overshoot	7 %	5%	2%	10%

FIG.6 SOURCE AND LOAD VOLTAGE WITHOUT DSTATCOM

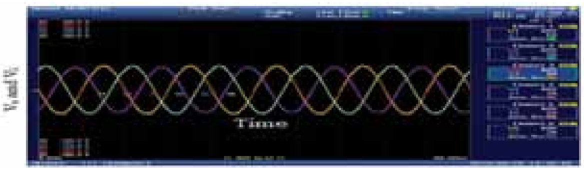

FIG.7 SOURCE AND LOAD VOLTAGE WITH DSTATCOM

FIG.8 THD WITHOUT DSTATCOM

5.0 CONCLUSIONS

Developed a prototype of DSP (Digital signal processor) controlled Distribution Static Synchronous Compensator (DSTATCOM) for 4 bus RDS capable of voltage regulation using Digital signal processor TMS320F2812. The experimental result demonstrates that the compensator effectively compensates Voltage sags and harmonic components of the non-linear loads.

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